AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions of claims in the application:

Listing of Claims:

1. (Currently Amended) A memory device comprising:

an array of memory formations associated with lithographic features of a wafer surface, each memory formation comprising[[;]] :

a first electrode formed from a bit line of the wafer;

two second electrodes ~~positioned sideways~~ in parallel orientation with respect to ~~of~~ the first electrode on walls of adjacent lithographic features of the wafer surface, to form two memory bits for one lithographic feature; and

a selectively conductive media placed between the first electrode and each one of the second electrodes, the first electrode operable with each of the second electrodes to selectively activate a memory portion of the selective conductive media.

2. (Currently amended) The memory device of claim 1, each second electrode ~~being~~ is substantially vertical and stacked laterally next to a side of the first electrode.

3. (Currently amended) The memory device of claim 1, the selectively conductive media comprises ~~atleast~~ at least one of a passive material and an organic material.

4. (Original) The memory device of claim 3, the organic material is a polymer.

5. (Original) The memory device of claim 3, the first electrode is operative with the second electrode as to activate a memory portion of the organic material.

6. (Currently amended) The memory device of claim 1, the selectively conductive material is ~~being~~ formed by a depositing system.

7. (Original) The memory device of claim 1, the first electrode formed according to a single or dual damascene process.

8. (Withdrawn) A method for fabricating a memory cell comprising:
providing a wafer having a bit line electrode with a raised surface above a substrate layer;
forming a selectively conductive layer over the raised surface and the substrate layer;
forming a top electrode layer over the selectively conductive layer; and
etching a surface to form a lithographic feature with a wall comprising a formed memory cell thereupon, the formed memory cell having the bit line electrode associating with two adjacent memory elements, each memory element including portions of the selective conductive layer and the top electrode layer.

9. (Withdrawn) The method according to claim 8, associating with two adjacent memory elements further comprises selectively activating a portion of the memory element.

10. (Withdrawn) The method according to claim 8, etching a surface further comprises etching a surface of the top electrode layer or a surface of the selectively conductive layer.

11. (Withdrawn) The method according to claim 8, etching a surface further comprises etching a surface of the bit line electrode.

12. (Withdrawn) The method according to claim 8, further comprising;
etching a surface of the selective conductive layer before forming the top electrode layer.

13. (Withdrawn) The method according to claim 8, etching a surface of the selective conductive layer further comprises a CMP process.

14. (Withdrawn) The method according to claim 8, further comprising:
forming a barrier layer to mitigate diffusion of the first electrode and the top electrode into a layer.

15. (Withdrawn) The method according to claim 8, further comprising:

forming the selectively conductive layer by a chemical vapor deposition process.

16. (Withdrawn) The method according to claim 8 further comprising:

forming at least one word line to access one or more of the memory cells fabricated in accordance with claim 8.

17. (Withdrawn) The method according to claim 8, further comprising forming a Cu_2S layer.

18. (Withdrawn) The method according to claim 8 further comprising forming the selective conductive layer and the top electrode layer by gas phase reaction process.

19. (Withdrawn) The method according to claim 8 further comprising forming a partitioning component next to the top electrode layer.

20. (Currently amended) A memory device comprising:

means for forming two memory elements on sidewalls of a lithographic feature, comprising:

means for forming first and second electrodes in a parallel direction with respect to a third electrode; and

means for sharing ~~an~~ the third electrode between the two memory elements.

21. (Currently Amended) A memory arrangement comprising:

a ~~single~~ first electrode operable with ~~two other~~ second and third electrodes positioned sideways and oriented parallel thereof, to form two memory elements for one lithographic feature on a wafer surface, each memory element comprising a selective conductive material that is sandwiched between the ~~single~~ first electrode and one of the ~~two other~~ second and third electrodes.

22. (Currently amended) The memory arrangement of claim 21, the second and third electrodes each ~~of the two electrodes~~ comprising at least one of aluminum, chromium, copper, germanium, gold, magnesium, manganese, indium, iron, nickel, palladium, platinum, silver, titanium, zinc, alloys thereof, indium-tin oxide, polysilicon, doped amorphous silicon, and metal silicides.